A Signal Distributor for Electronic Switching Systems

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The purpose, design and operation of the signal distributor are described in this paper. The signal distributor is the unit in the experimental electronic switching system which is used to distribute action signals. A semiconductor gate selector, driving a large group of memory flip-flops is used to generate the necessary action signals from a high-speed binary address. Factors governing the design are outlined and some alternate solutions compared.

I. INTRODUCTION

The signal distributor is the means of distributing action signals in the experimental electronic switching system (Fig. 1). The central control processes the necessary information, employing high-speed low-power electronic circuits. The signal distributor converts the high-speed low-power signals received from the central control into low-speed high-power signals required for certain operations in the system. The control of supervision or dial pulsing in trunk circuits constitutes the major part of these operations, and control of various maintenance circuits within the administration center is one of the other miscellaneous operations in the electronic switching system that is performed by the signal distributor.

The signal distributor consists of a selector driving a large group of flip-flops with associated amplifiers (Fig. 2). The amplifiers have sufficient power capacity to operate relays where necessary. The flip-flops permit output signals of long duration. They act as memory elements, accepting two high-speed signals from the selector which designate the starting and ending times of the output signal. The selector performs the translation of a binary address received from the central control.

II. FUNCTIONAL REQUIREMENTS

The binary address is presented to the signal distributor as a particular combination of potentials on 21 address leads (Fig. 2). Twenty of

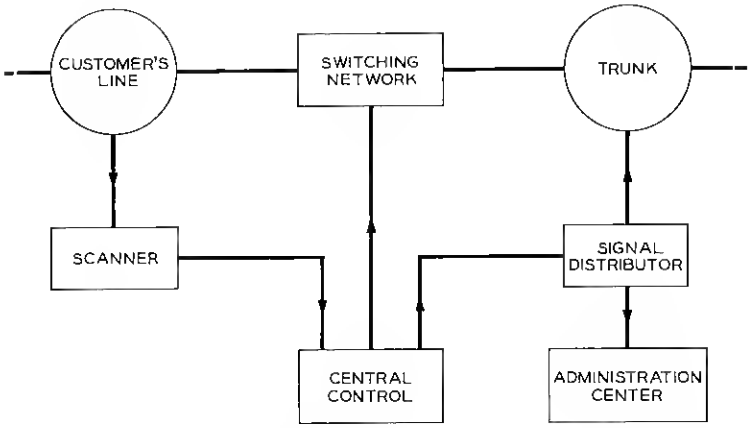

Fig. 1 — Simplified block diagram of an experimental electronic switching system.

these leads are grouped in ten pairs, the 21st is the enable lead. The potentials on any of the ten pairs are always conjugate: if one of the leads in a pair is at ground potential or in the passive state, the other will be at a positive potential or in the active state. Consequently, each pair can assume two distinctly different states and, for the ten pairs of address leads, there are $2^{10} = 1024$ possible combinations of potentials. A combination is assigned to every order. The order must be carried out by the signal distributor whenever the particular combination appears on the ten pairs of address leads and the enable lead becomes active.

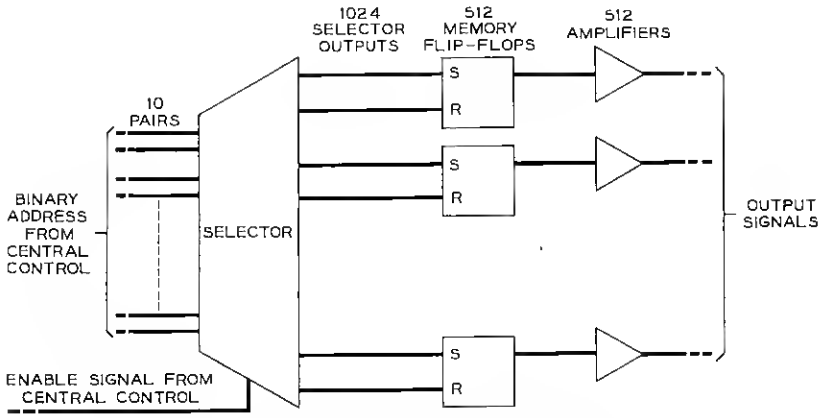

Fig. 2 — Functional diagram of the signal distributor.

For the control of each slow-speed output signal path two orders are necessary, one to start a particular action and another to terminate it. Therefore, the 1024 available combinations or addresses are sufficient to control 512 different output signal paths. After receiving the binary address, the selector must produce an active signal, suitable for activating a memory flip-flop, on one out of 1024 leads. This is a process of combinational logic and is commonly known as binary to one-out-of-n translation.

Various devices and circuits can be employed to accomplish the translation. A particular design, however, must be compatible with the power levels available at the inputs and required at the outputs. It also must be able to respond to the fastest expected address repetition rates. Furthermore, the most economical design that still meets the basic requirements and is sufficiently reliable should be attempted.

The input or address signals to the selector are presented by transistor amplifiers in the central control. Antisaturating techniques are used in these amplifiers, which limit their current carrying capacity to 30 milliamperes. Also, because of antisaturating circuits, the amplifier outputs never return to an exact ground potential in the passive state. The potential in the active state is limited by the breakdown voltage of the transistors used. An active potential of 16 volts is considered a safe value.

The fastest expected address repetition rate is 7.5 microseconds. This means that the potentials on at least one pair of address leads may be reversed every 7.5 microseconds. Under certain conditions the potentials on all ten pairs may be reversed at this rate. The selector must be able to accept addresses and produce an active output on one of its 1024 output leads every 7.5 microseconds. Furthermore, the memory flip-flops should be able to change their states within this time.

The memory flip-flops in the signal distributor are of the same design as those used in the logic circuitry of the central control. They require a 5-milliampere current pulse for less than a microsecond on their input leads for setting or resetting. The memory flip-flops themselves have limited output-power capacity. A single-transistor amplifier is provided at the output of each flip-flop. The transistor in this amplifier is allowed to saturate, thus permitting comparatively large currents to be switched. In fact, with proper protection against inductive surge voltages, relays can be operated directly from the amplifier output. The amplifier also serves as a buffer between the output load and the memory flip-flop. The output loads may vary widely, depending upon the nature of the connected circuitry.

The outputs of the signal distributor have to operate various types of relays as well as different slow-speed electronic circuits. For the type of memory flip-flop used in the signal distributor, it is essential that there always be a constant load on the flip-flop outputs. If this load is permitted to vary, the operation of the flip-flop will be seriously affected. The normal driving pulse may not be sufficient to set or reset the flip-flop, or it may be impossible to change the state of the flip-flop at all. The amplifier presents a constant load to the flip-flop, independent of the load variations to the amplifier. In this way, the requirements on the output signal of the selector are the same for all 1024 selector outputs. The output signal of the selector must be sufficient to change the state of the memory flip-flop. A current pulse of 5 milliamperes amplitude is required, and it must overcome a threshold of about 5 volts, which threshold is built into the flip-flop to guard against triggering from noise. The pulse must exist at the input terminal of the flip-flop for at least 0.3 microsecond to assure positive triggering.

III. DESIGN CONSIDERATIONS OF THE SELECTOR

Because of the input and output power levels, as well as the required address repetition rates, semiconductor gates are best suited for performing the function of binary to one-out-of-n translation in the signal distributor. The required repetition rate of 7.5 microseconds is sufficiently low to permit the use of saturating transistor circuits wherever amplification is necessary. Saturating circuits can switch larger currents than can circuits using antisaturating techniques, and they are simpler and more efficient. The gates can employ either transistors or diodes, and can be arranged in a single or multistage pattern.

In deciding whether transistors or diodes should be employed as gates, and how many stages of logic should be used, certain contradicting factors must be considered and a compromise solution found. In general, the number of devices should be minimized. In doing this, the relative cost and reliability of diodes versus transistors must be taken into account. Multistage logic reduces the number of gates, but it may require interstage amplifiers to compensate for loss of level. The total dc power consumption is an important factor; in large translators this can be greatly reduced by using resistors as gate elements and applying voltages only on the gates that are active at a given time. For a practical design, particularly one that is to be used in a telephone office, it is highly desirable to keep the number of different circuit units to a minimum. As the number of stages is increased, more different

circuit units are required. This complicates maintenance problems, particularly if replaceable plug-in type circuit units are to be used. A single-stage translator using diodes as gate elements and transistors as drivers or amplifiers has the advantage of simplicity. Only two different circuit units are required, because all the gates are the same, and there is no need for interstage amplification. For translators of small size, single-stage logic is the preferred solution.

There are definite practical limitations to single-stage diode translators. These limitations become increasingly more pronounced as the size of the translator increases. The number of diodes required in a single-stage diode translator is $n2^n$, where n is the number of binary digits. For a ten-bit single-stage translator, 10,240 diodes are needed. Another limiting factor is the input-to-output current ratio or fanout. In order to provide a certain current at the active output, each driving circuit at the input must be able to switch $(2^n - 1)/n$ times that current. At the inputs of a ten-bit translator, a current 102 times larger than the active output current must be switched. This would require considerable amplification of the available input signals. The dc power that must be supplied to a single-stage diode translator is 2^n times the power required for one active output.

For translators of four binary bits and larger the number of diodes can be reduced by various arrangements of multistage logic. The fanout and dc power can be reduced by using either transistor or resistor-diode gates in place of straight diode gates. The selector of the signal distributor employs diodes and resistors as gate elements in a two-stage logic, with transistors being used in amplifier circuits to provide gain where necessary. Compared to a single-stage logic diode translator, the circuit is considerably more economical. The number of diodes is reduced from 10,240 to 1,344, the required dc power is 32 times smaller and the input fanout is decreased from 102.3 to 6.2.

Small additional savings in the number of diodes can be obtained by introducing a three-stage logic. This, however, would require a few more different circuit units. Not only would the total number of units be larger, the necessity of keeping spares for all types of circuit units used in a device would actually increase the number of diodes that have to be provided.

Within the framework of the outlined specific requirements, and considering the limitations of available devices, the design of the selector is an optimum with respect to the number and cost of devices, as well as to power consumption. Reliability can only be estimated when more data is available on the relative failure rates of transistors and diodes.

IV. DESIGN OF THE SELECTOR

The two-stage selector of the signal distributor (Fig. 3) may be considered as consisting of the following basic building blocks: (a) primary translators, (b) enable circuit, and (c) secondary translator, or 32 x 32 matrix.

4.1 *Primary Translators*

The first stage of translation has two identical five-bit diode translators. Five pairs of input leads, or half of the address, are connected to each primary translator. Each translator selects and activates one out of 32 output leads corresponding to the binary input. The translators

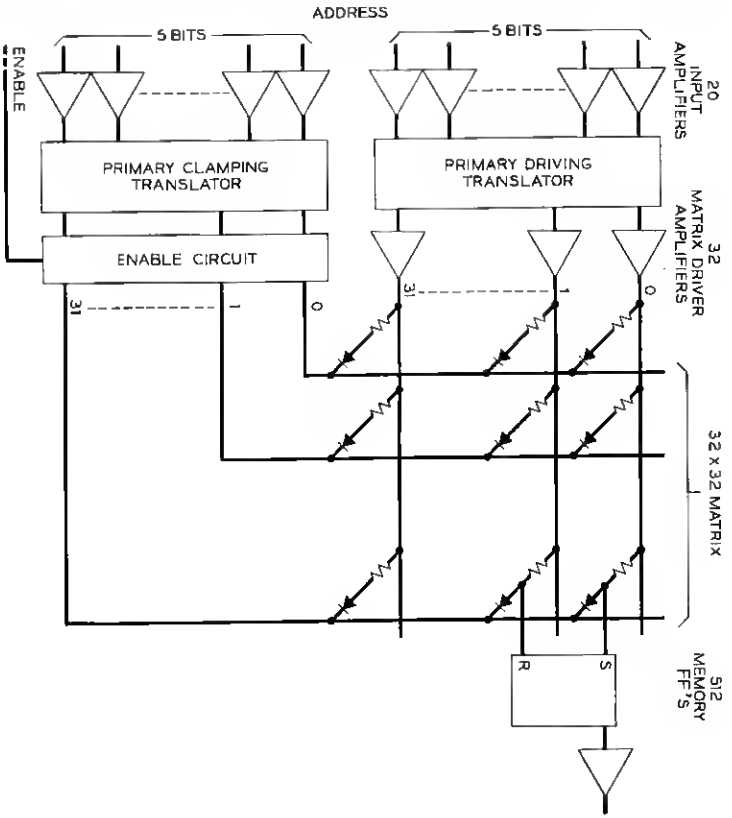

Fig. 3 — Block diagram of the signal distributor.

themselves consist of 160 diodes, five diodes for every output. The diodes are connected in an AND gate logic pattern.

At each input of the primary translators, a transistor amplifier or switch is provided. These amplifiers provide a low-impedance discharge path for the connecting cable capacitance. In this way, a regular switchboard cable can be used to transmit the fast-changing address signals from the central control to the signal distributor. The amplifiers also restore the voltage level of the address signals and provide a current sink at the inputs of the primary translators. The transistors in these amplifiers are allowed to saturate, thus introducing about 1.5 microseconds delay during the transition from the passive to the active state. This delay is mainly due to the storage time. The delay from the active to the passive state is only about 0.5 microsecond; this difference in transfer times is very desirable for the proper operation of the primary translators. It means that, whenever a pair of input leads is reversing its state, there is a time of about 1 microsecond when both leads are passive. This prevents any undesired outputs from the translator while the input address is changing.

The outputs of the two primary translators are used to operate the second-stage translator or the 32 x 32 matrix. Because of the nonsymmetrical two-input resistor-diode AND gate used in the matrix, the outputs of the two primary translators have to perform different functions. One of the primary translators has 32 amplifiers connected to its outputs, with each amplifier at an active output applying a 22-volt source to one of the inputs of the 32 x 32 matrix. The amplifiers are called matrix drive amplifiers, and the primary translator is designated the driving translator.

The other primary translator applies a ground clamp to 32 inputs of the matrix. Whenever an output of this translator becomes active, the ground clamp is removed from the corresponding matrix lead. This translator is called the clamping translator. All the 32 outputs of the clamping translator are normally kept at ground level by the enable circuit. Only after the enable circuit removes its ground from the 32 output leads can the active output remove the ground clamp from the selected matrix input.

4.2 *Enable Circuit*

The enable circuit prevents any active signals from the clamping translator reaching the matrix. A certain time after the enable circuit receives an active enabling signal from the central control, it allows the

signal to pass from the clamping translator to the matrix. The main purpose of this delay is to avoid false operations. When the address to the primary translators is changed, the selected output of the clamping translator becomes active before the previously active output of the driving translator disappears. The reason for this is the time delay in the matrix drive amplifiers. These amplifiers have to supply a comparatively heavy current to the matrix so that two stages of saturating transistors must be used. The time delay relationship of the outputs of the two primary translators is indicated in Fig. 4. If the active output from the clamping translator were permitted to pass to the matrix immediately, an undesired gate in the matrix would be activated. The enable circuit releases the clamping translator outputs 5 microseconds after the change of the input address, thus allowing sufficient time for the previously active matrix drive amplifier to reach the passive state. The clamping translator is released for 2 microseconds, which is sufficient time to change the state of the memory flip-flop.

The enable circuit must generate a delayed and stretched signal upon receiving the enable pulse from the central control. The circuit in Fig. 5

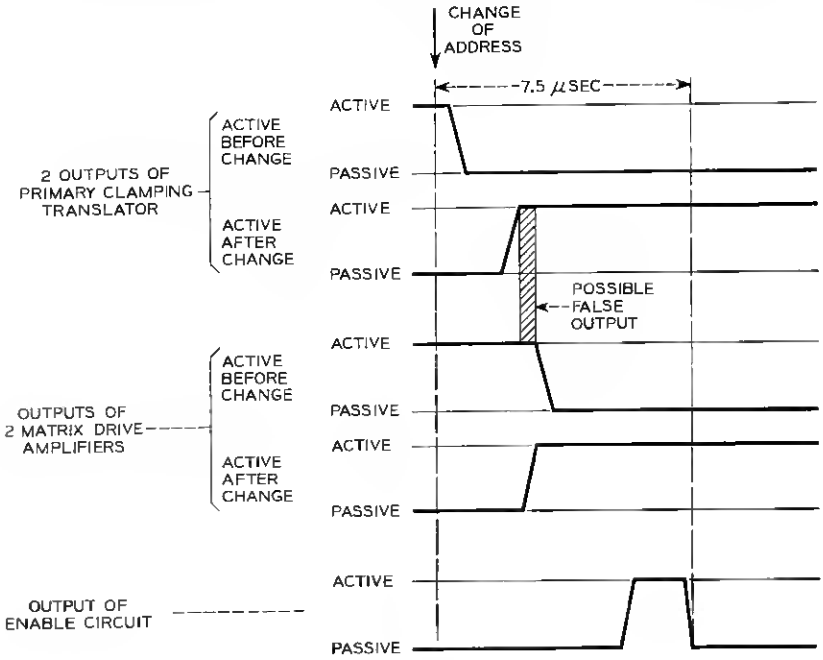

Fig. 4 — Time relations.

performs this function. The enable pulse arrives from the central control on a coaxial cable and, at the same time, the address is changed on the ten pairs of input leads. The cable must be properly terminated, because the enable pulse is only 0.3 microseconds long. Two self-resetting flip-flops are used to provide the timing; the first is set by the enable pulse and resets itself after 5.0 microseconds, with the trailing edge of its output setting the second flip-flop. This flip-flop resets after two microseconds; its output (after proper amplification) is used to enable the primary clamping translator. All 32 outputs of the clamping translator are provided with an extra diode each. The diodes are normally grounded by the amplifier of the delay circuit. When the delayed 2-microsecond signal arrives, the ground is removed and the active signal can pass from the clamping translator to the matrix.

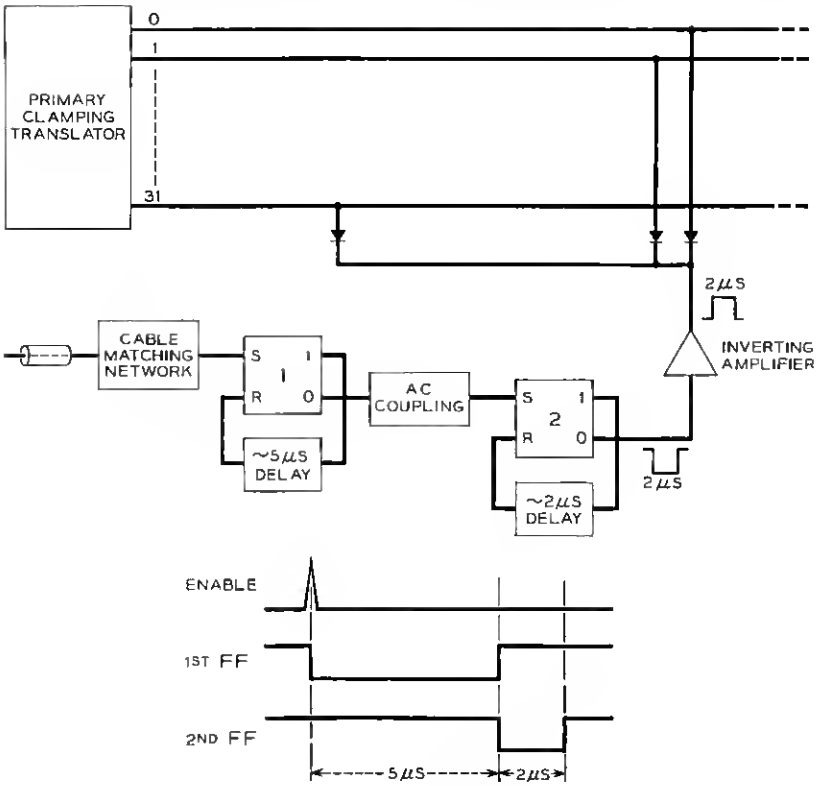

Fig. 5 — Enable circuit.

4.3 *Secondary Translator or 32 x 32 Matrix*

The second-stage translator may be considered as a 32 x 32 matrix consisting of 1024 resistor-diode AND gates. Simultaneous application of potential on the resistor and removal of ground from the diode is necessary to produce an output from the gate. An active matrix-driver amplifier applies 22-volt potential to a group of 32 resistors and the active output of the clamping translator removes ground from 32 diodes. There is only one gate that is common to both groups; in this, the current will flow from the matrix driver amplifier through the gate resistor into the memory flip-flop and change its state.

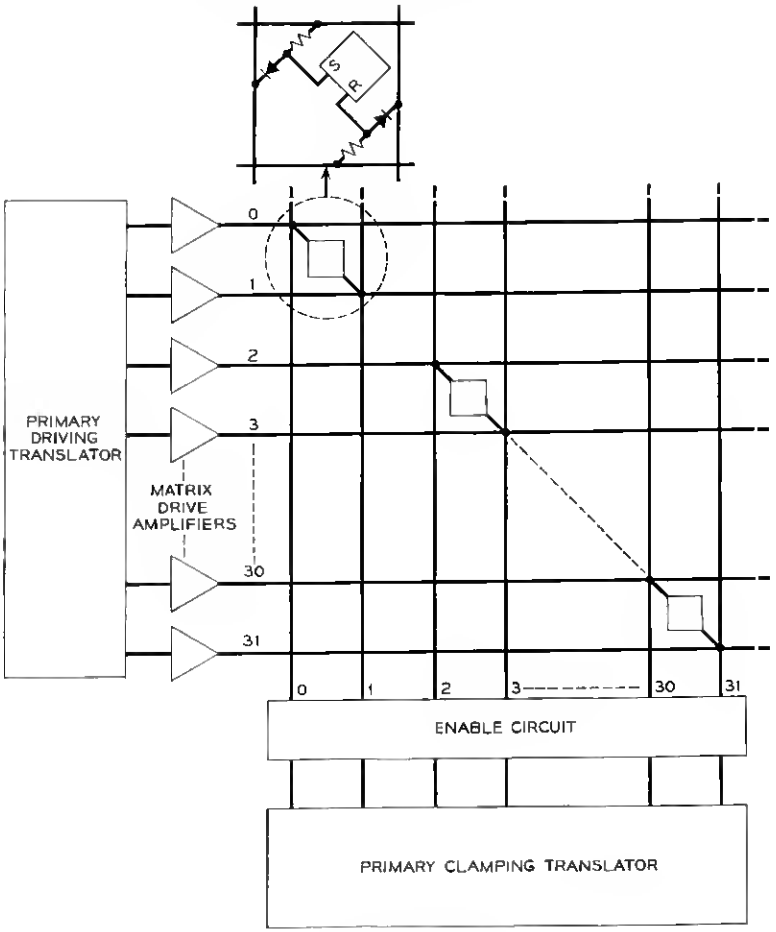

Fig. 6 — Test flip-flops.

V. TESTING AND MAINTENANCE

Every design of telephone switching equipment must provide sufficient reliability; a situation where failure of a component would disable the whole system cannot be tolerated. A total failure of the signal distributor would seriously affect the system. Not only would signaling on trunks be impossible, but many important testing and maintenance functions could not be carried out.

To insure reliability of the signal distributor, certain critical circuits are provided in duplicate and connected by relay contacts in such a way that one can be interchanged for the other in case of failure. Also, preventive maintenance can be performed in the standby circuit, greatly reducing the chance of failure. Only circuits in which a failure would disable more than one output are duplicated. Such circuits are the primary translators with the input amplifiers, the enable circuit and the matrix-drive amplifiers. Any failure within these circuits would disable at least

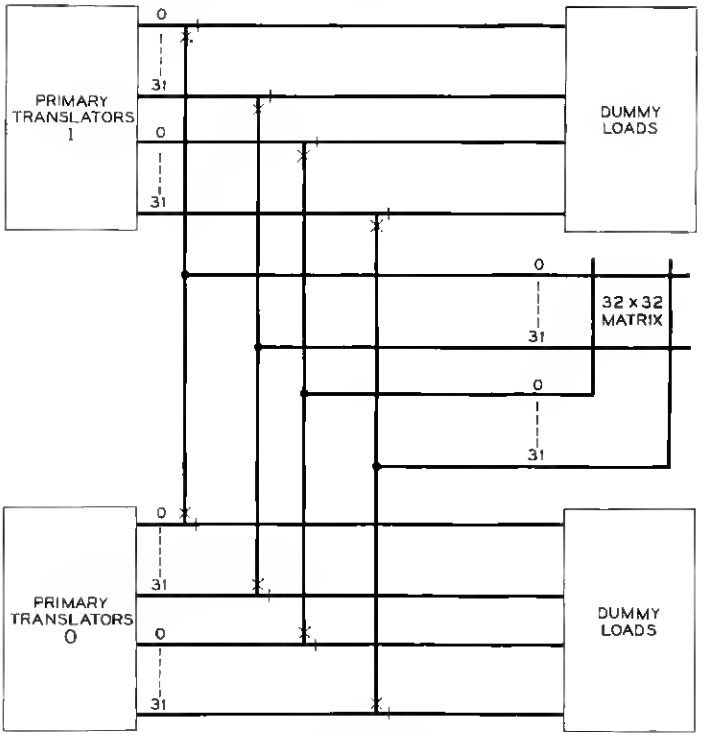

Fig. 7 — Transfer circuit.

Fig. 8 — Signal distributor cabinet.

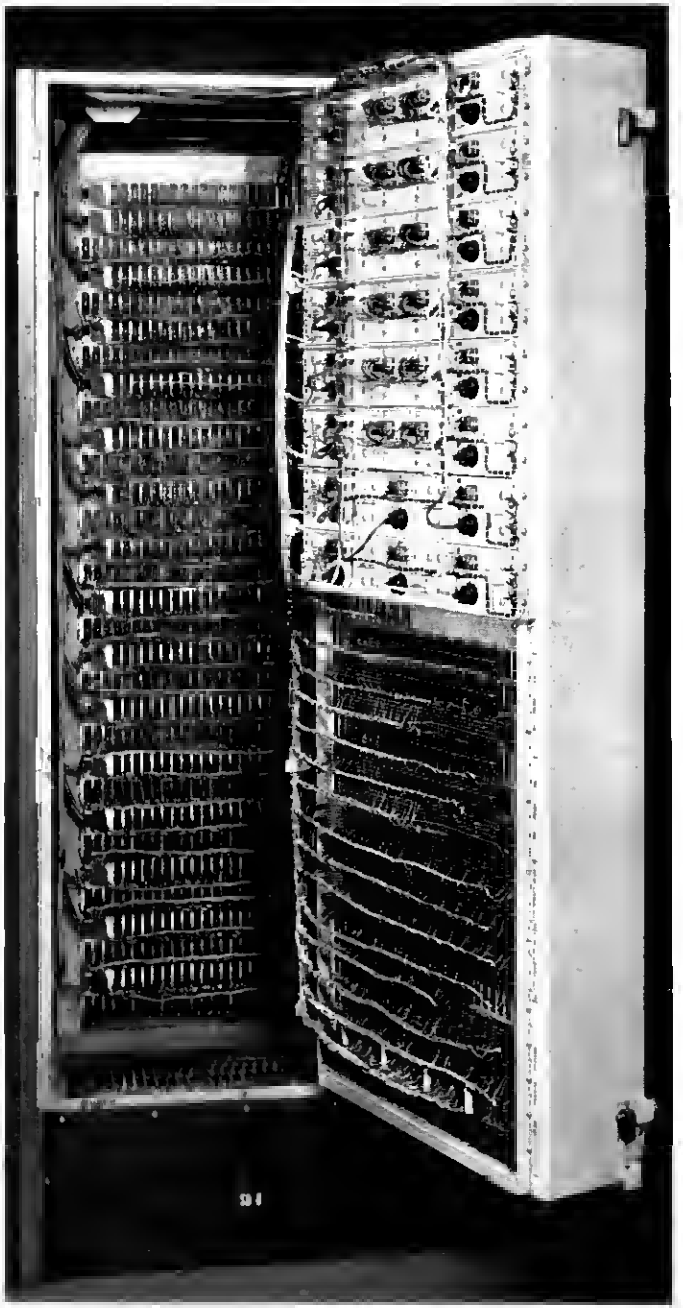

Fig. 9 — Cabinet with gate open

32 output points. A single failure within the 32 x 32 matrix or a memory flip-flop, however, would affect only one output point. This is not considered serious and these circuits are not duplicated.

Before a standby circuit can be switched into operation, a failure of the active circuit must be recognized. For this purpose, a test routine is performed. At certain intervals the central control sends a sequence of addresses to the signal distributor to test its proper operation. Sixteen test flip-flops are connected at the outputs of both primary translators in such a way that they will detect an improper response of any of the outputs (Fig. 6). The central control observes the outputs of the test flip-flops by means of the scanner. Immediately after a failure is recognized, the faulty units are switched out of service and replaced by standby units. The standby units are also tested at regular intervals to assure that they are in operating condition. The actual switching of duplicated units is accomplished by relay contacts (Fig. 7). Interlock and sequencing circuits are provided, assuring continuity of clamping voltages. The same relays also apply dummy loads to the standby units in order to test them under loaded conditions. To prevent false outputs, no addresses are sent to the signal distributor during the switching operation.

Each of the duplicated units has its own power supply. Failure of a supply will be recognized as a failure of the whole circuit and the standby unit will be switched in. The rectifiers for the duplicated circuits are fed

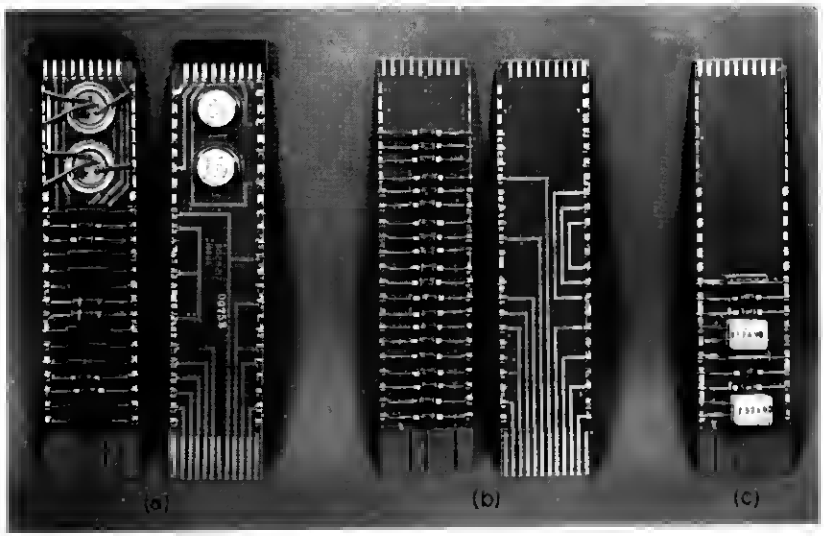

Fig. 10 — Typical circuit units.

from independent ac supplies, assuring continuity in case of an ac power failure. The continuity of power in the nonduplicated part of the circuit is assured by paralleling rectifiers.

VI. EQUIPMENT

The signal distributor is a self-contained unit. All the electronic circuits, power supplies and transfer relays are mounted in one enclosed cabinet. Fig. 8 shows the cabinet with front door open. The individual power supplies, duplicated primary translators and transfer relays are mounted on a swinging gate. Opening the gate (Fig. 9) provides for easy access to the terminals and wiring. The back of the cabinet contains all the output flip-flops with associated amplifiers.

The electronic circuits are mounted as units on replaceable printed wiring boards. Fig. 10 shows three typical circuit units: (a) is the transistor flip-flop used as the output memory element, with a shorting shoe provided to facilitate testing of the transistors outside of the circuit; (b) contains only diodes and constitutes part of the primary translator, the whole five-bit translator consisting of eight similar units; (c) is the coaxial cable terminating network.

The circuit units are slot-coded and plug into appropriate jacks. They can be easily replaced without interrupting operation of the unit. A centralized repair service of defective units is anticipated. This, together with the automatic trouble location, should greatly simplify the maintenance of the electronic switching system.

VII. ACKNOWLEDGMENTS

The equipment concepts which are the basis for the signal distributor design as well as the common control and scanner are the result of many contributions, notably those of H. A. Miloche and H. J. Wirth, Jr. The specific equipment design of the signal distributor was done by A. A. Nehez.